**EE 465 Lab1**

**The code:**

module lab1(iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1, oRESULT);

input iCLK, iRST\_N, iSEL;

input iA0, iA1, iB0, iB1;

output oRESULT;

wire iCLK, iRST\_N;

wire [7:0] iA0, iA1, iB0, iB1;

reg [16:0] oRESULT;

always @ (posedge iCLK) begin

if(iRST\_N)begin

if(iSEL) begin

oRESULT <= iA0 \* iB0 + iA1 \* iB1;

end

else begin

oRESULT <= iA0 \* iB0 + iA1 \* iB1 + iA0 \* iA1 \* iB0 \* iB1;

end

end

else begin

oRESULT <= 0;

end

end

endmodule

**Testbench Code:**

`timescale 1ns/10ps

module lab1\_tb ();

reg iCLK\_t, iRST\_N\_t, iSEL\_t;

reg [7:0] iA0\_t, iA1\_t, iB0\_t, iB1\_t;

wire [16:0] oRESULT\_t;

lab1 X(iCLK\_t, iRST\_N\_t, iSEL\_t, iA0\_t, iA1\_t, iB0\_t, iB1\_t, oRESULT\_t);

initial begin

iCLK\_t = 0;

iRST\_N\_t = 0;

iSEL\_t = 0;

iA0\_t = 0;

iA1\_t = 0;

iB0\_t = 0;

iB1\_t = 0;

end

always #1 iCLK\_t = ~iCLK\_t;

always

#2 begin

if(iA0\_t == 127)

iA0\_t = 0;

else

iA0\_t = iA0\_t + 1;

end

always

#4 begin

if(iA1\_t == 127)

iA1\_t = 0;

else

iA1\_t = iA1\_t + 1;

end

always

#8 begin

if(iB0\_t == 127)

iB0\_t = 0;

else

iB0\_t = iB0\_t + 1;

end

always

#16 begin

if(iB1\_t == 127)

iB1\_t = 0;

else

iB1\_t = iB1\_t + 1;

end

always #32 iSEL\_t = ~iSEL\_t;

always #64 iRST\_N\_t = ~iRST\_N\_t;

endmodule

Simulation:











